
How to Apply AI in Semiconductor Manufacturing

: Current Approaches and Case Studies



2024.08.09

Data Mining & Quality Analytics Lab.

이영환

발표자 소개



❖ 이영환(Youngwan Lee)

- 고려대학교 일반대학원 산업경영공학과 재학
- Data Mining & Quality Analytics Lab.(김성범 교수님)
- 석사과정(2023.03 ~)

❖ 연구 관심 분야

- Image Segmentation, Anomaly Detection
- AI in Semiconductor Industry, Smart Factory

❖ E-mail

- lyh0105@korea.ac.kr

❖ Introduction

- 인공지능의 발전과 제조업 수요 증가
- 인공지능의 제조업 활용 방안과 인공지능의 도입을 어렵게 하는 요소들
- 반도체 공정이란?

❖ Paper Review

- Case Study : 반도체 제조공정 인공지능 적용 연구 7개 분야 대표논문 살펴보기

❖ Summary & Conclusion

1. Introduction

Introduction

Rapid Growth of Artificial Intelligence

➤ 최근 인공지능은 양적으로, 질적으로 급격한 발전을 이루고 있음



Artificial Intelligence Index Report 2024
Stanford University
Human – Centered Artificial Intelligence)

전세계적으로 출판된 영어권 인공지능 논문 수 (단위: 1000건)

인공지능 시스템의 벤치마크 별 성능 (vs. human baseline)

Number of AI publications in the world, 2010–22

Source: Center for Security and Emerging Technology, 2023 | Chart: 2024 AI Index report

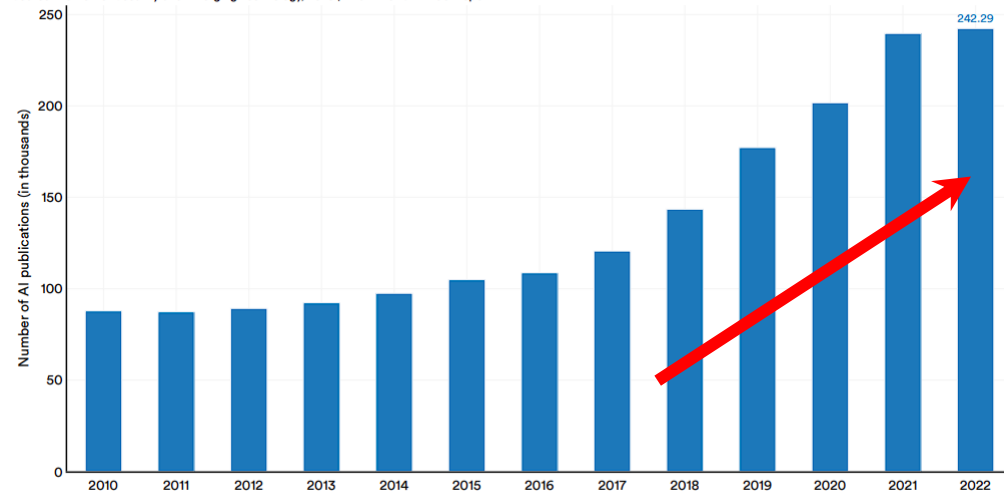


Figure 1.1.1

Select AI Index technical performance benchmarks vs. human performance

Source: AI Index, 2024 | Chart: 2024 AI Index report

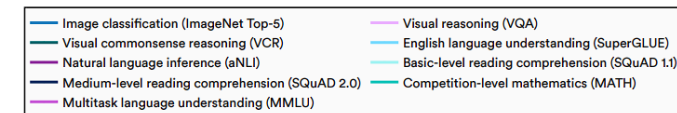
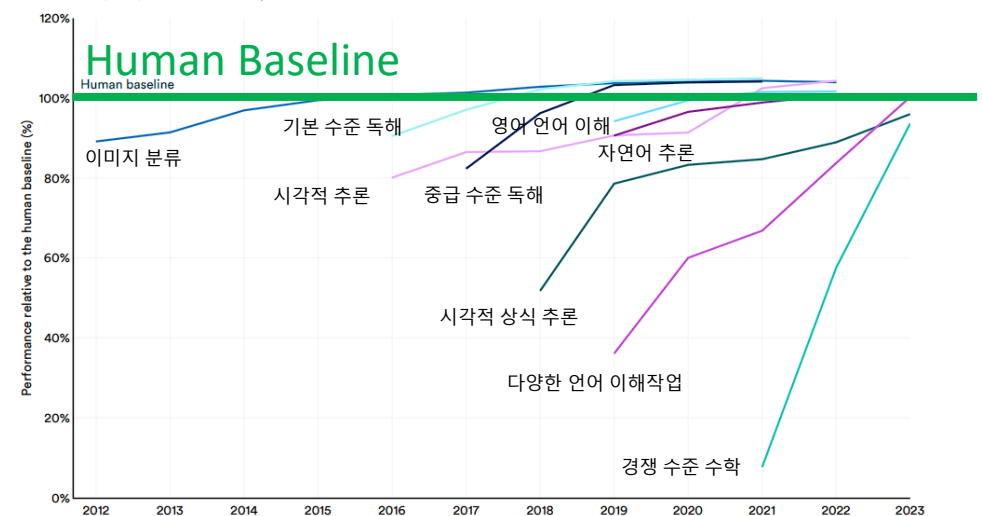
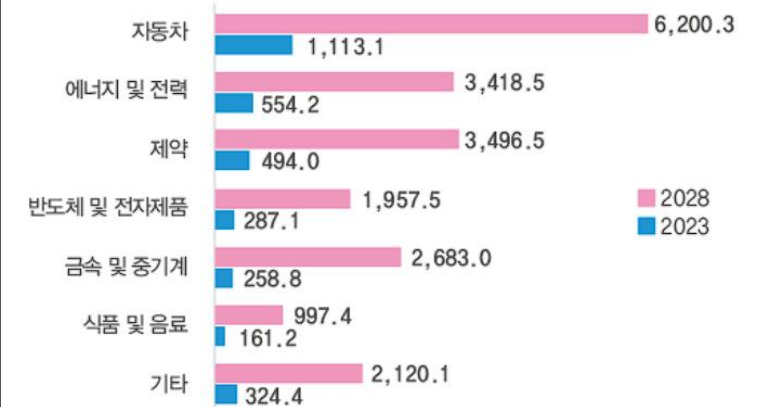
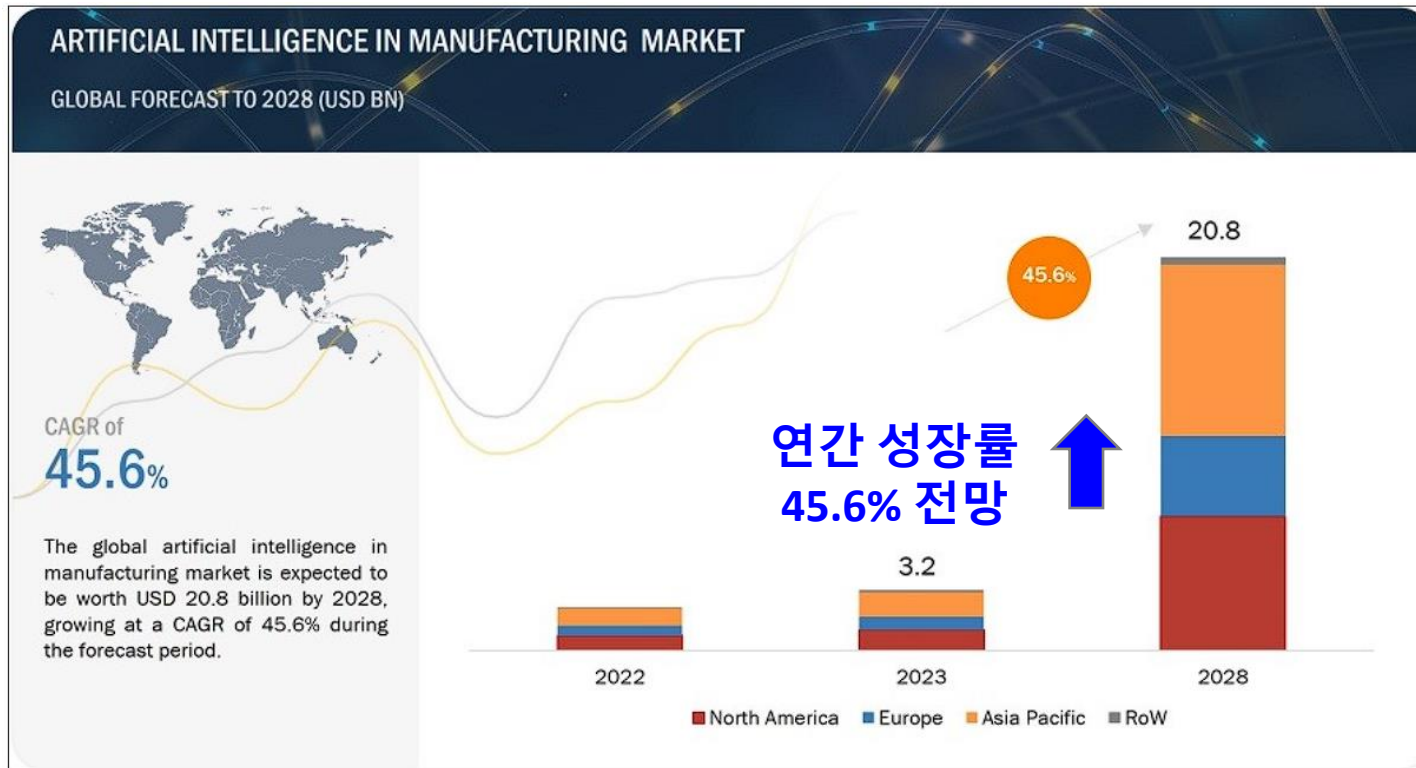


Figure 2.1.16*

Introduction

Increasing Demand for Artificial Intelligence in Manufacturing

- 각 산업계는 인공지능의 활용을 통한 수익화 방안에 대해 고민 중이며, 제조업에서도 인공지능에 대한 수요 증가 중



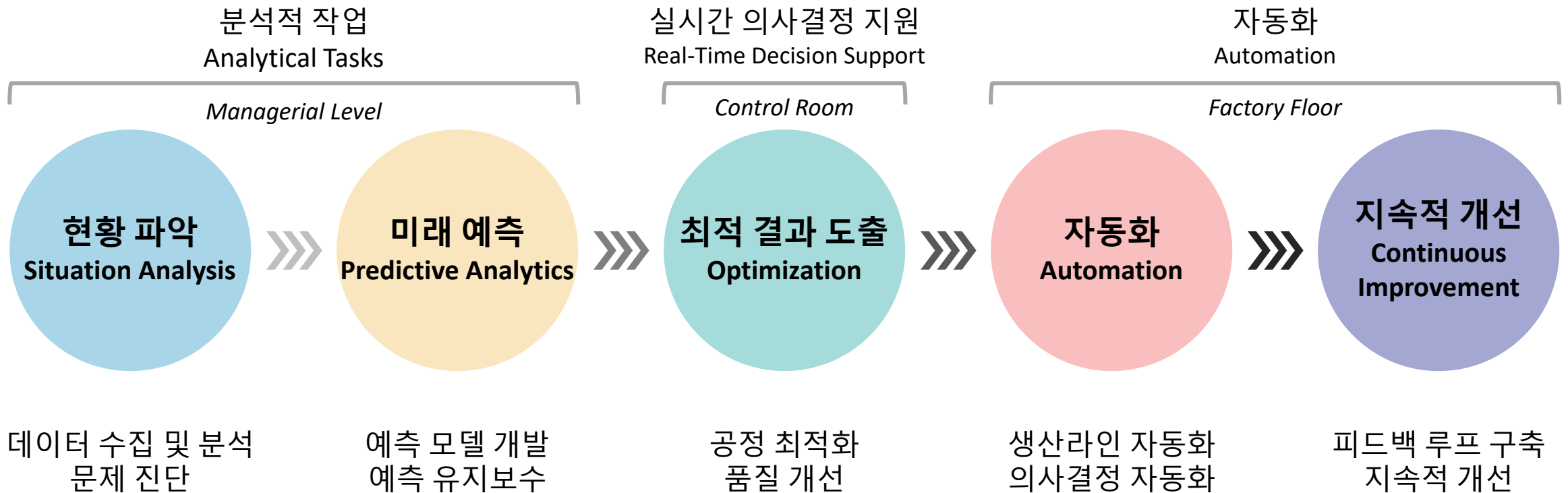
<https://www.marketsandmarkets.com/Market-Reports/artificial-intelligence-manufacturing-market-72679105.html>

<http://webzine.koita.or.kr/202403-specialissue/%EC%A0%9C%EC%A1%B0%EC%97%85-AI-%ED%99%9C%EC%9A%A9-%EC%A0%84%EB%A7%9D>

Introduction

AI/ML Solutions for each application

- 인공지능은 제조업에 어떤 형태로 활용이 가능할까?



※ 출처논문 Figure 6 재구성

Introduction

Challenges involved in implementing AI/ML solutions within the manufacturing industry

➤ 제조업에 인공지능 적용을 어렵게 하는 요소는?

데이터 수집 Data Acquisition

- Expensive labeled data
- Sparse, noisy, and missing sensor measurements

에너지 소비 Energy Consumption

- AI/ML training has large energy footprint
- Powering AI/ML enabled edge devices

보안 Security

- Data centers exposed to malicious attacks
- Employee privacy concerns during data collection

구현 Implementation

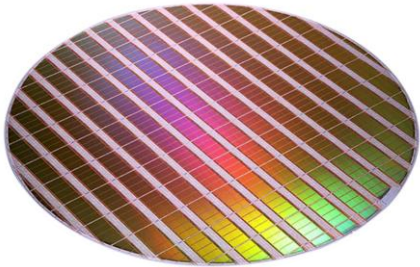
- Recruiting necessary expertise
- Building trust in AI/ML solutions

※ 출처논문 Figure 5 & Table 1 재구성

Introduction

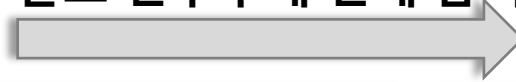
Application of AI in Semiconductor Manufacturing

➤ 반도체 제조공정 분야 인공지능 주요 연구주제는?



2022년 이후

발표 연구주제 전체 탐색



IEEE TRANSACTIONS ON
SEMICONDUCTOR
MANUFACTURING

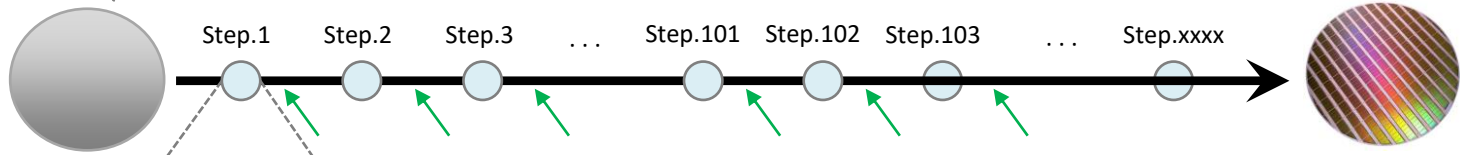
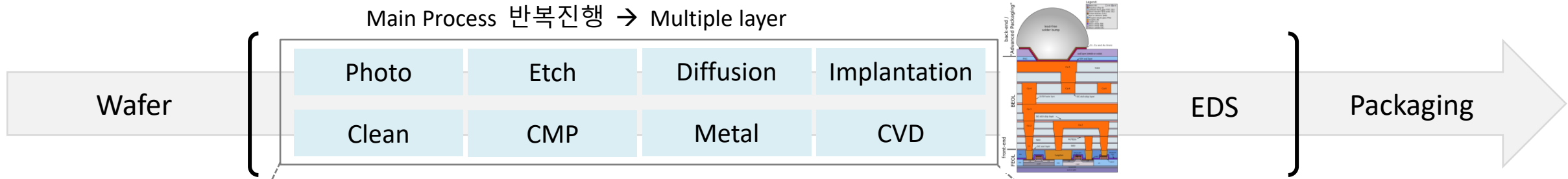
ASMC
ADVANCED
SEMICONDUCTOR
MANUFACTURING
CONFERENCE

1. 공정 최적화
2. 설비 예지보전
3. 설비 스케줄링
4. 부품 잔존수명 예측
5. 원인인자 분석 & 수율 예측
6. 웨이퍼 맵
7. 검사/리뷰/분류

Introduction

A brief introduction to the Semiconductor Manufacturing Process

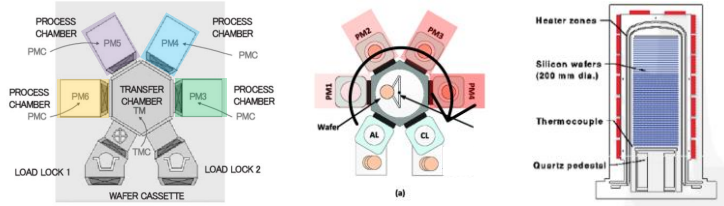
반도체 제조공정이란?



각 Main Process를 진행하는 여러 대의 설비가 존재함



1대의 설비 안에도 여러 개의 챔버/유닛 존재함 (공정/설비/메이커 별 상이)



1. Main Process (○)

- 공정 (Recipe)
- 설비 (FDC)

2. Metrology & Inspection (↗)

- 계측 (CD, THK, Overlay, 농도)
- 검사 & 리뷰

Introduction

DMQA Open Seminar

➤ 반도체 제조공정 관련 이전 세미나 참고

종료

Active Learning in Semiconductor Manufacturing

2021. 08. 20
Data Mining & Quality Analytics Lab.
발표자 : 황성진

Active Learning in Semiconductor Manuf:

발표자:  **황성진**

 2021년 8월 20일

 오후 1시 ~

 온라인 비디오 시청 (YouTube)


세미나 정보 보기 →


종료


Yield Prediction & Enhancement in the Semiconductor Manufacturing


이창현 2018.07.06

Yield Prediction & Enhancement in the S<

발표자:  **이창현**

 2018년 7월 6일

 오후 2시 ~

 고려대학교 신공학관 218호

세미나 정보 보기 →

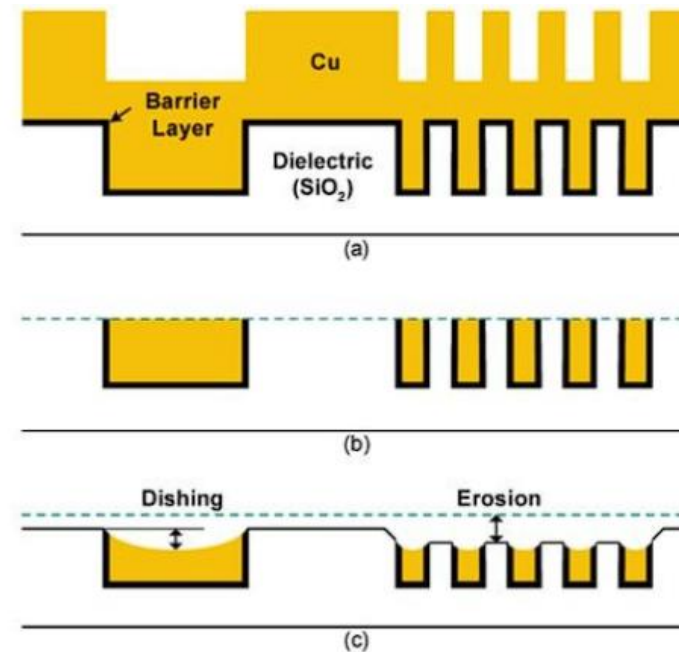
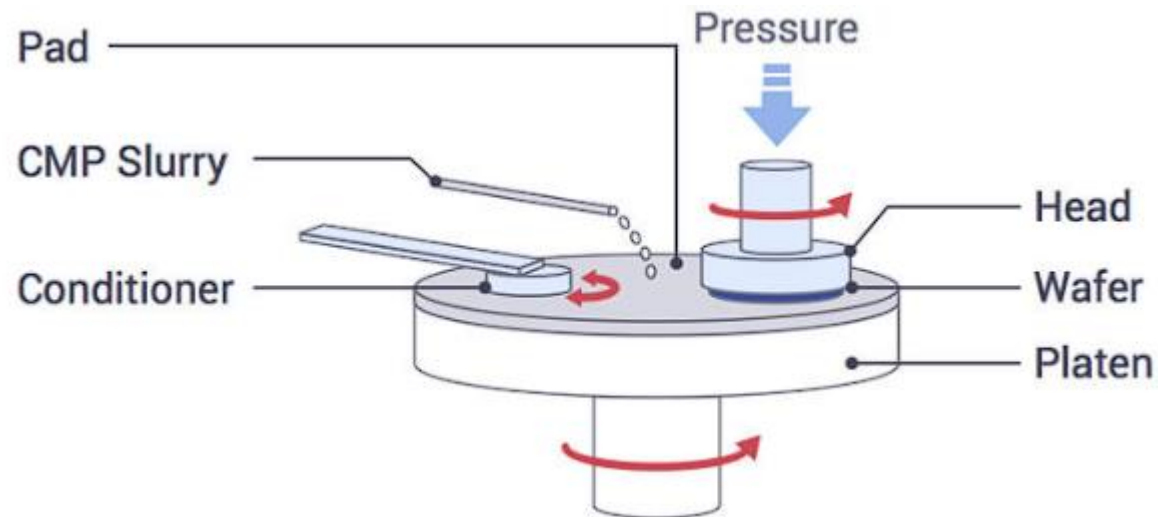
2. Paper Review – Case Study

1. 공정 최적화

주요 공정의 매개변수를 분석하고 최적화하여 생산 효율과 제품 품질 향상

- ❖ A Fine-Grained, End-to-End Feature-Scale CMP Modeling Paradigm Based on FCN (IEEE TSM, 2023)

CMP (Chemical Mechanical Polishing)



(a) CMP 공정 이전 Profile, (b) 이상적인 연마 이후 표면, (c) Dishing & Erosion

<https://sshmyb.tistory.com/225>

1. 공정 최적화

주요 공정의 매개변수를 분석하고 최적화하여 생산 효율과 제품 품질 향상

❖ A Fine-Grained, End-to-End Feature-Scale CMP Modeling Paradigm Based on FCN (IEEE TSM, 2023)

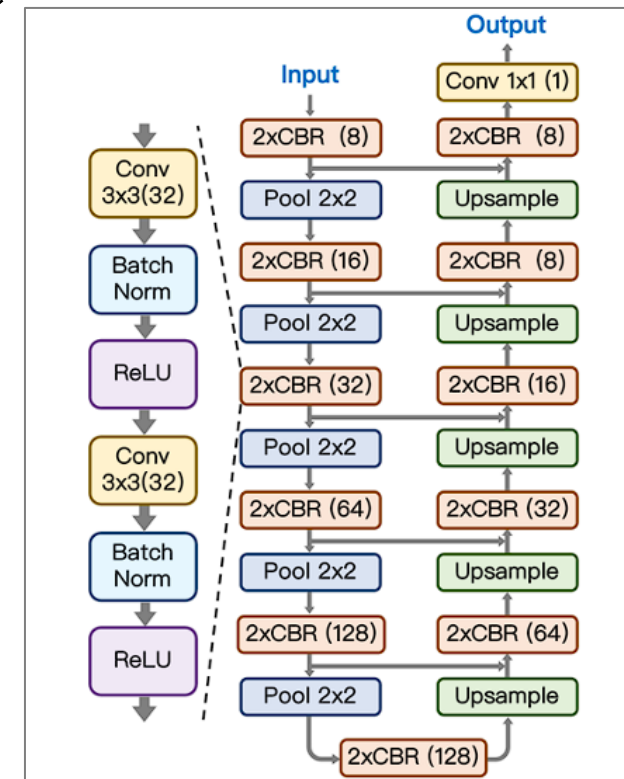
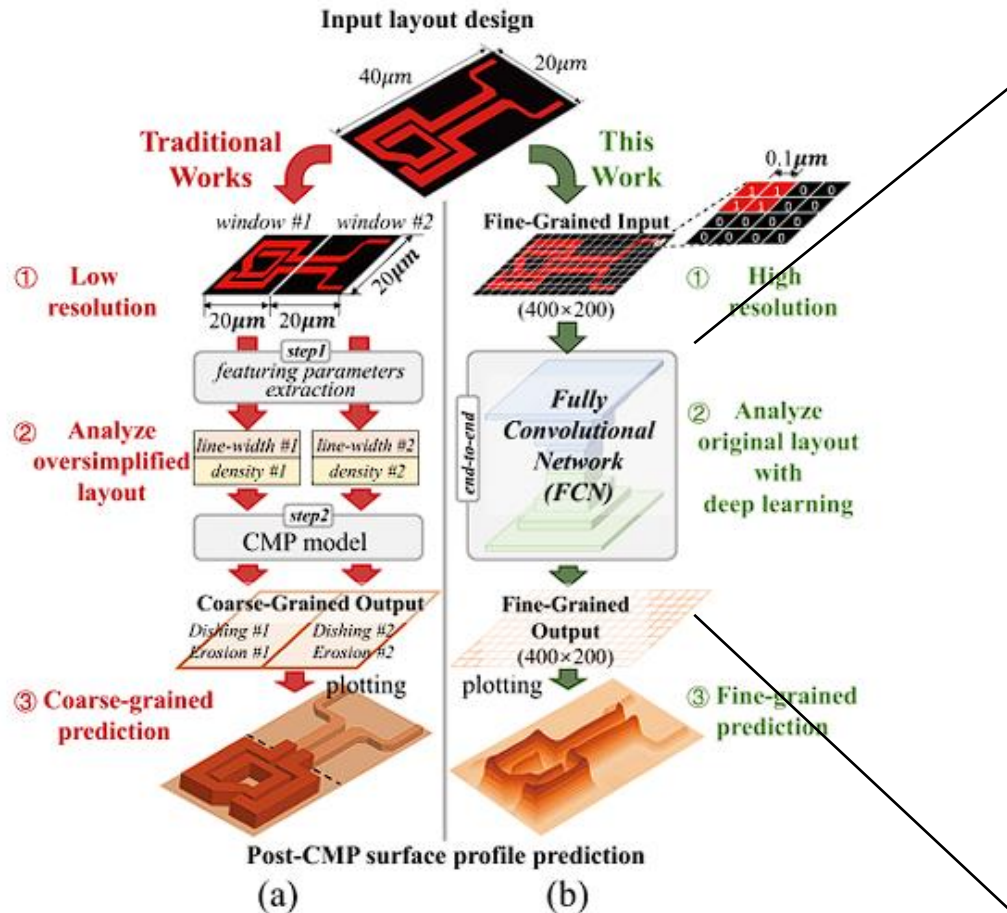


Fig. 3. Architecture of the fully convolutional neural network. Numbers in brackets represent the number of output channels (i.e., the number of kernels).

1. 공정 최적화

주요 공정의 매개변수를 분석하고 최적화하여 생산 효율과 제품 품질 향상

❖ A Fine-Grained, End-to-End **Feature-Scale CMP Modeling Paradigm Based on FCN** (IEEE TSM, 2023)

AFM 측정 방식

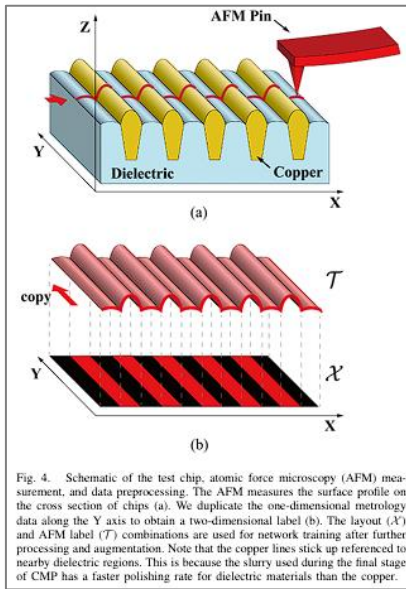


Fig. 4. Schematic of the test chip, atomic force microscopy (AFM) measurement, and data preprocessing. The AFM measures the surface profile on the cross section of chips (a). We duplicate the one-dimensional metrology data along the Y axis to obtain a two-dimensional label (b). The layout (X) and AFM label (Y) combinations are used for network training after further processing and augmentation. Note that the copper lines stick up referenced to nearby dielectric regions. This is because the slurry used during the final stage of CMP has a faster polishing rate for dielectric materials than the copper.

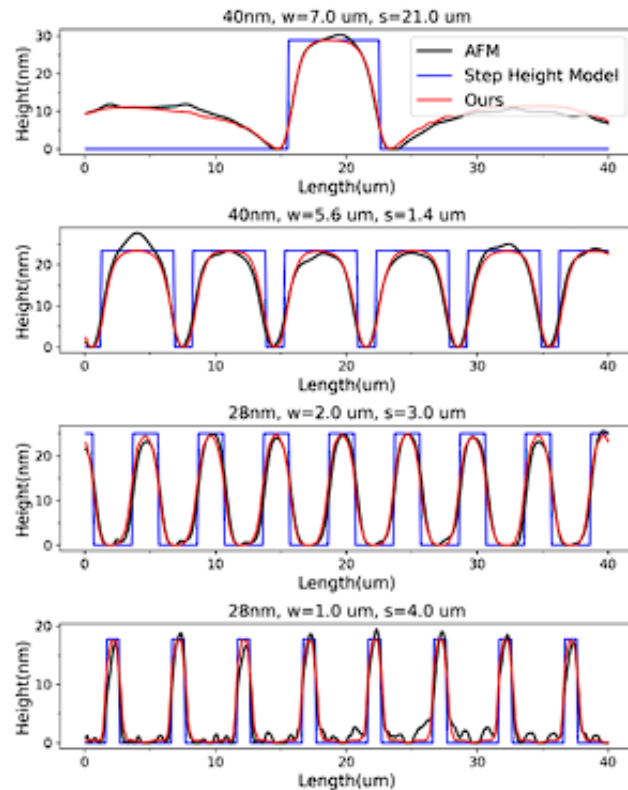


Fig. 5. A cross-sectional view of part of the model's prediction results. The ordinate denotes the surface's relative height, whereas the abscissa denotes its horizontal location. Under two process nodes and different combination of line-widths (w) and spacings (s), the proposed method could more accurately depict the chip's surface profile than the previous step height model.

TABLE I
TEST LOSS ON TWO PROCESS NODES

	40nm		28nm	
	L1(nm)	RMSE(nm)	L1(nm)	RMSE(nm)
Step Height Model	4.1935	6.2689	3.6601	5.5842
FCN model (ours)	1.0632 (0.0067)	1.4927 (0.0074)	1.2753 (0.0075)	1.9135 (0.0087)
Improvement	74.6%	76.2%	65.2%	65.7%

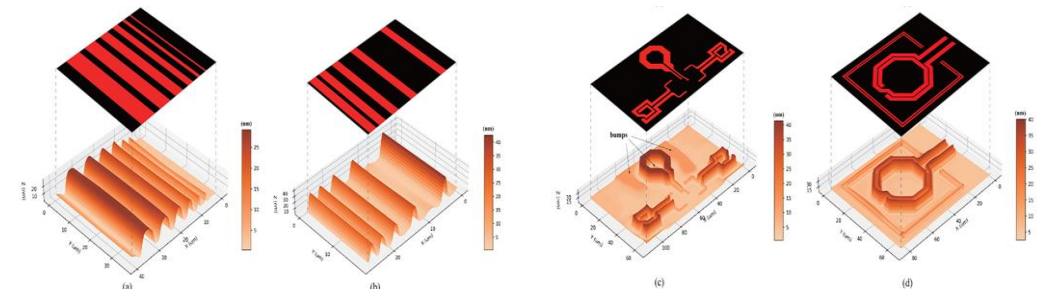


Fig. 6. Demonstration of micro-topography prediction. Patterns in red represent copper areas, while the black parts represent dielectric regions. The layout in (a) has the same spacing and different line-width, while the layout in (b) has different spacing and the same line-width. (c) and (d) are parts of two real-world analog IC designs under the 40 and 28 nm processes, respectively. Note that the Z and X,Y axes are in different scales, so the surface unevenness is highlighted in the figure.

1. 공정 최적화

주요 공정의 매개변수를 분석하고 최적화하여 생산 효율과 제품 품질 향상

❖ Machine Learning for Deep Trench Bottom Width Measurements using Scatterometry (ASMC, 2023)

✓ Training

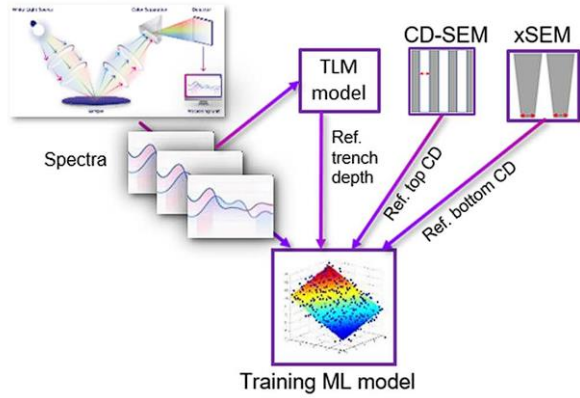


Fig. 1. Machine learning model building scheme.

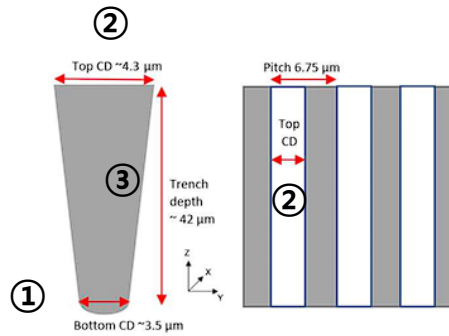


Fig. 3. Schematic image representing side and top view of the 2D line trenches.

<Side View> <Top view>

✓ Inference

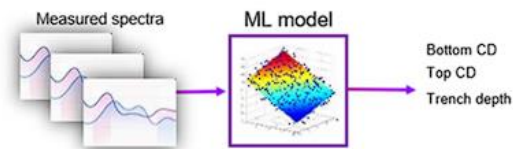


Fig. 2. Machine learning model deployment to obtain parameters of interest from measured spectra.

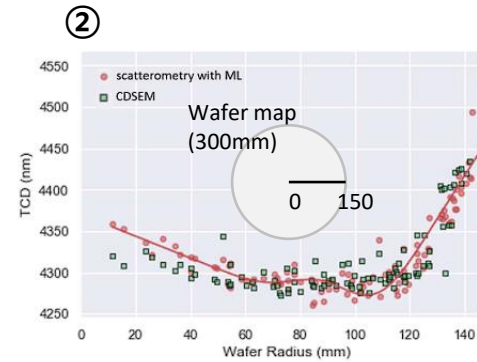


Fig. 5. Top CD of the line trench POR wafer as a function of wafer radius, comparing CD-SEM (green square symbols) and scatterometry measurements using the ML method (red circles).

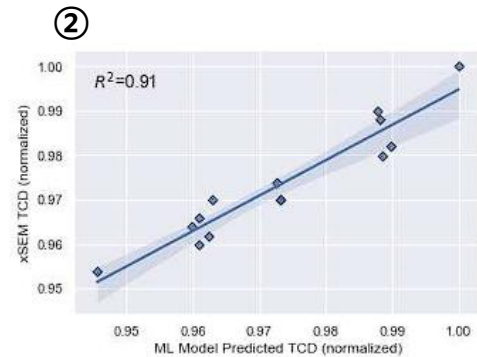


Fig. 13. Circular trench top CD measured in SEM cross-sections is plotted versus scatterometry measurements using the ML method. The SEM cross-section data were not used in the training set.

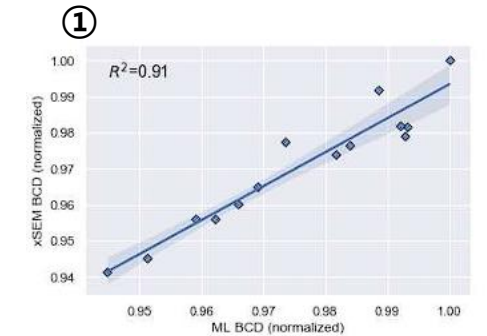


Fig. 10. Circular trench bottom CDs obtained from cross-sections are plotted versus values obtained from Leave-One-Out Cross-Validation (LOOCV). 14 cross-sections were made from the split group of 7 wafers.

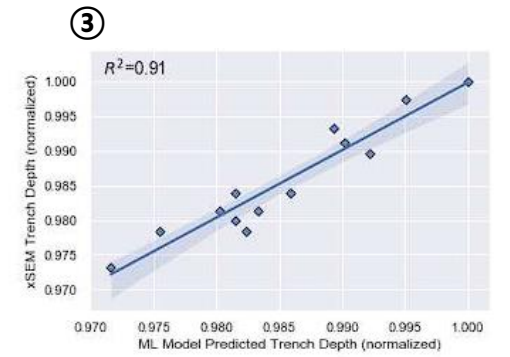


Fig. 14. Circular trench depth obtained from SEM cross-sections is plotted versus scatterometry results using the ML method. The SEM cross-section data were not used in the training set.

2. 설비 예지보전

설비 센서데이터를 통해 주요 인자의 거동이나 고장을 예측하고 사전 조치를 통해 가동 중단으로 인한 손실 최소화

- ❖ Effective **Variational-Autoencoder-Based Generative Models** for Highly **Imbalanced Fault Detection Data** in Semiconductor Manufacturing (IEEE TSM, 2023)

PECVD (Plasma Enhanced Chemical Vapor Deposition)

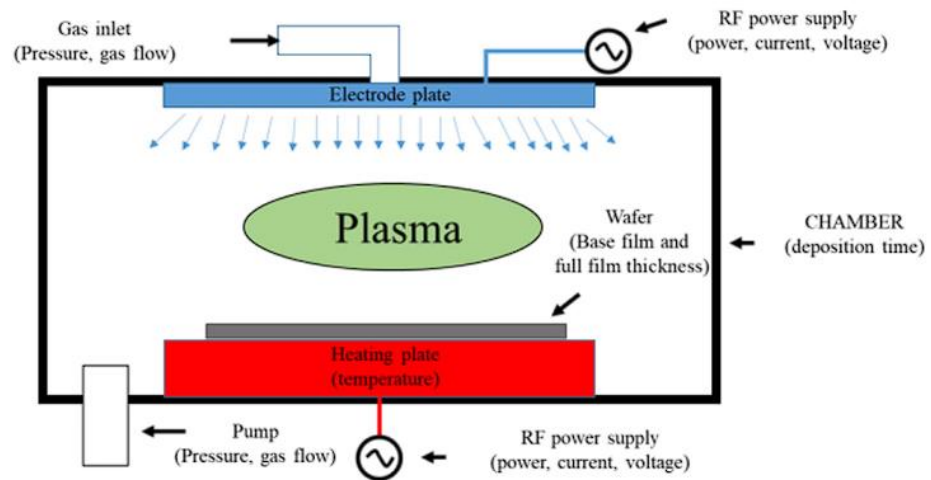


Fig. 1. Plasma enhanced chemical vapor deposition (PECVD).

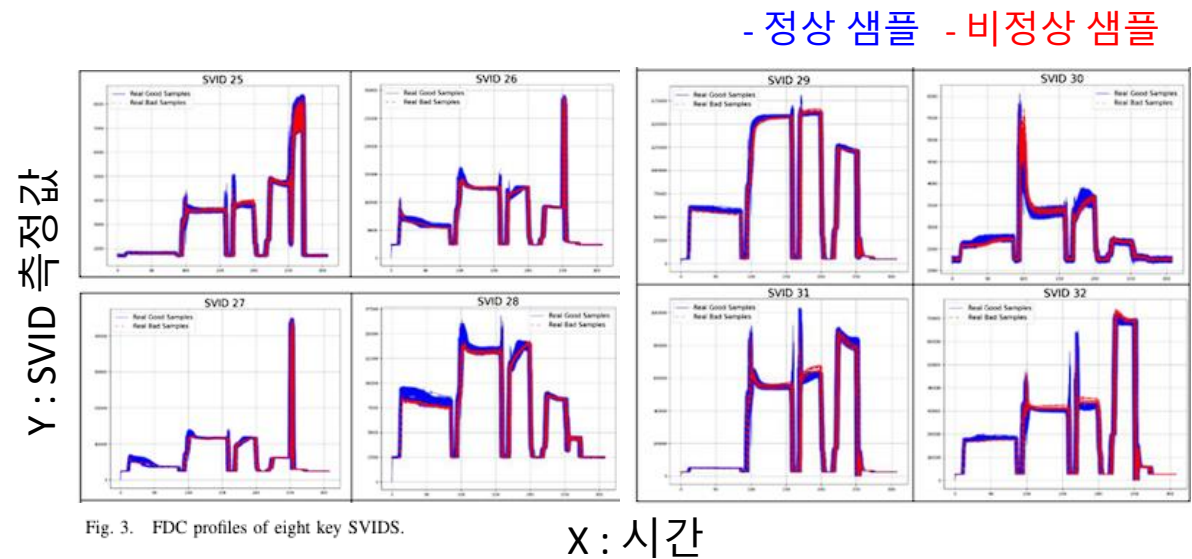


Fig. 3. FDC profiles of eight key SVIDs.

Status Variable Identification (SVID)

- 공정 상태 모니터링하고 이상 징후 감지
- 공정 개선, 품질 관리, 예지 보전 등의 목적으로 분석됨
- 데이터 불균형 : 소수의 결함 샘플 + 다수의 정상 샘플

2. 설비 예지보전

설비 센서데이터를 통해 주요 인자의 거동이나 고장을 예측하고 사전 조치를 통해 가동 중단으로 인한 손실 최소화

❖ Effective Variational-Autoencoder-Based Generative Models for Highly Imbalanced Fault Detection Data in Semiconductor Manufacturing (IEEE TSM, 2023)

2가지 데이터 구성 전략

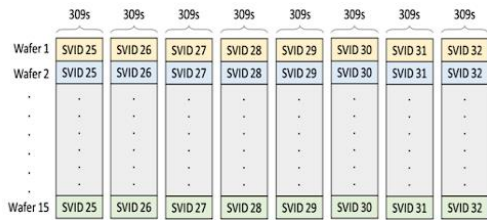


Fig. 5. The Individual strategy.

각 SVID를 독립적으로 처리 → 데이터 증강
: 데이터의 독립성 유지

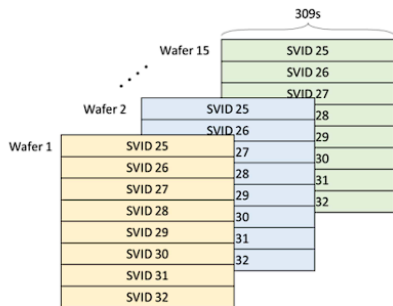


Fig. 6. The Concatenation strategy.

여러 SVID를 결합하여 처리 → 데이터 증강
: 데이터 간 상호작용 고려

VAE Model을 통한 데이터 생성 : 데이터 불균형 문제 해결

결합 샘플의 잠재 변수 추출

새로운 결합 샘플 생성

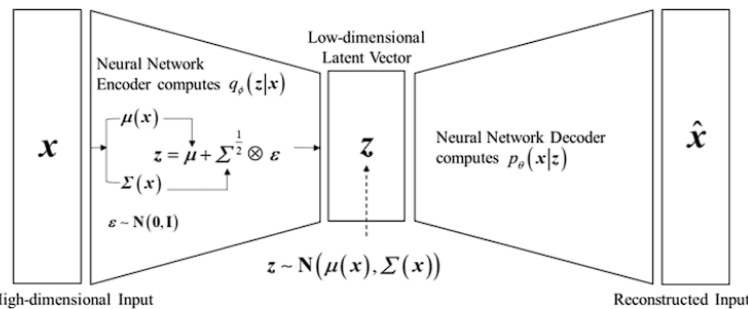


Fig. 2. General architecture of a VAE model.

- 정상 샘플 - 비정상 샘플(데이터 증강)

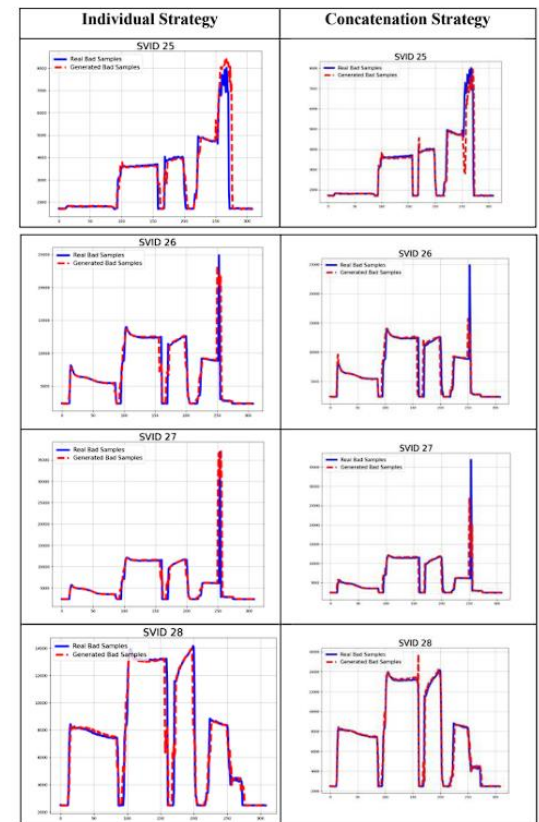


Fig. 10. Generated temporal profiles of abnormal wafers for SVIDs 25-28 via the VAE models.

2. 설비 예지보전

설비 센서데이터를 통해 주요 인자의 거동이나 고장을 예측하고 사전 조치를 통해 가동 중단으로 인한 손실 최소화

- ❖ Effective **Variational-Autoencoder-Based Generative Models** for Highly **Imbalanced Fault Detection** Data in Semiconductor Manufacturing (IEEE TSM, 2023)

기본모델 - 분류 성능

TABLE I
PRELIMINARY CLASSIFICATION EVALUATION WITHOUT DATA AUGMENTATION

Classifier	Evaluation Metrics				
	Accuracy	Precision	Recall	F ₁ -score	Specificity
Random Forests	95.44%	100%	58.06%	73.47%	100%
AdaBoost	96.63%	100%	69.03%	81.68%	100%
Bagging	95.09%	100%	54.84%	70.83%	100%
XGBoost	94.60%	100%	50.32%	66.95%	100%

AdaBoost + 데이터 증강

TABLE III
PERFORMANCE EVALUATION OF ADABOOST USING THE INDIVIDUAL STRATEGY

Original + Generation	Evaluation Indicators				
	Accuracy	Precision	Recall	F ₁ -score	FNR
15	96.63%	100%	69.03%	81.68%	30.97%
133	97.37%	100%	75.81%	86.24%	24.19%
266	98.21%	100%	83.55%	91.04%	16.45%
399	97.93%	100%	80.97%	89.48%	19.03%
532	100%	100%	100%	100%	0%
665	100%	100%	100%	100%	0%

XGBoost + 데이터 증강

TABLE IV
PERFORMANCE EVALUATION OF XGBOOST USING THE INDIVIDUAL STRATEGY

Original + Generation	Evaluation Indicators				
	Accuracy	Precision	Recall	F ₁ -score	FNR
15	94.60%	100%	50.32%	66.95%	49.68%
133	98.21%	100%	83.55%	91.04%	16.45%
266	98.67%	100%	87.74%	93.47%	12.26%
399	99.44%	100%	94.84%	97.35%	5.16%
532	98.35%	100%	84.84%	91.80%	15.16%
665	98.21%	100%	83.55%	91.04%	16.45%

제안된 VAE 기반 데이터 증강 방법은

- ✓ 불균형한 Fault Detection을 효과적으로 처리하고
- ✓ 분류 성능을 크게 향상시킴을 통해 결함 감지 능력 향상시킴

3. 설비 스케줄링

각 설비의 가동 일정을 최적화하여 생산라인의 효율성을 높이고, 병목현상을 줄여 품질하락을 막고 생산 시간 단축

❖ Practical Reinforcement Learning for Adaptive Photolithography Scheduler in Mass Production (IEEE TSM, 2024)

포토공정 – Track Stepper System을 통해 연속적으로 이루어짐
기존의 규칙기반 스케줄링은 복잡한 제조환경에서 비효율적

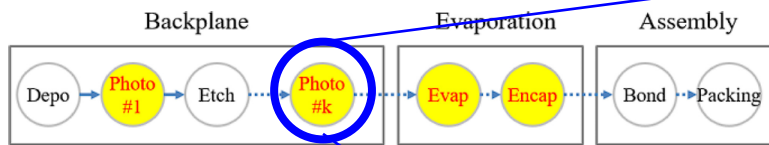


Fig. 1. Manufacturing process of AMOLED. The photo k-steps appear in multiple patterned layers of the backplane process. The bottleneck steps are represented with yellow color in general context.

- ✓ 반도체/디스플레이 제조공정에서 **포토리소그래피** 공정은 대표적으로 병목현상이 일어나는 공정



<https://news.skhyunx.co.kr/post/circuit-patterns-in-ultra-fine-regions>

3. 설비 스케줄링

각 설비의 가동 일정을 최적화하여 생산라인의 효율성을 높이고, 병목현상을 줄여 품질하락을 막고 생산 시간 단축

❖ Practical Reinforcement Learning for Adaptive Photolithography Scheduler in Mass Production (IEEE TSM, 2024)

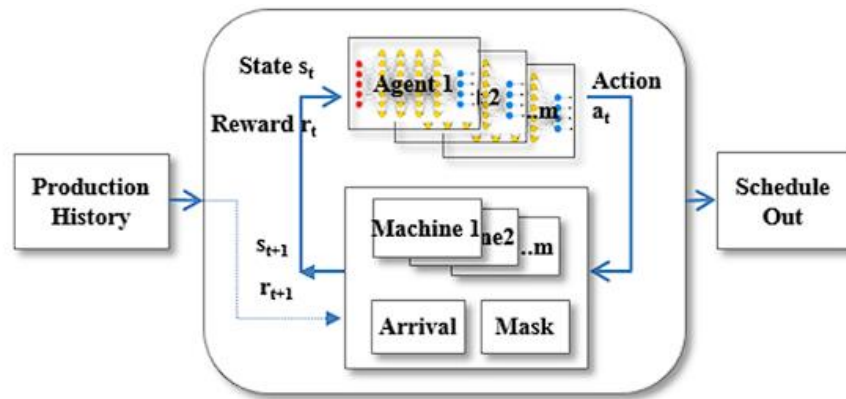


Fig. 2. Reinforcement learning scheduler modeling for photolithography machines.

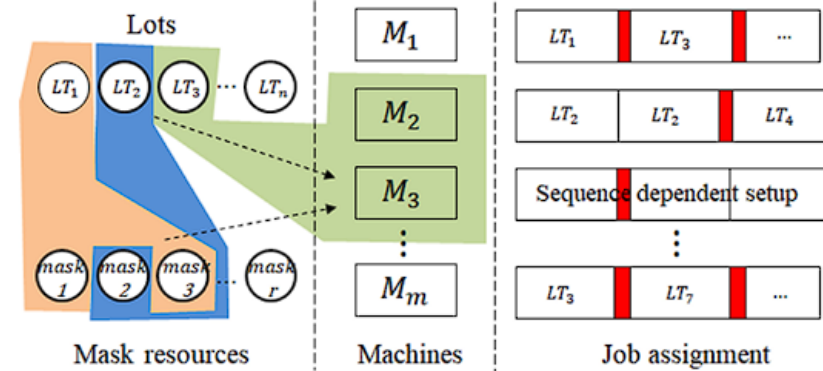


Fig. 3. Illustration of scheduling for m parallel machines, n types of lots and r masks. Typical lots are constraint to multiple masks and machines. The machines share the masks and setup time is required according to the job assignment sequence.

3. 설비 스케줄링

각 설비의 가동 일정을 최적화하여 생산라인의 효율성을 높이고, 병목현상을 줄여 품질하락을 막고 생산 시간 단축

❖ Practical Reinforcement Learning for Adaptive Photolithography Scheduler in Mass Production (IEEE TSM, 2024)

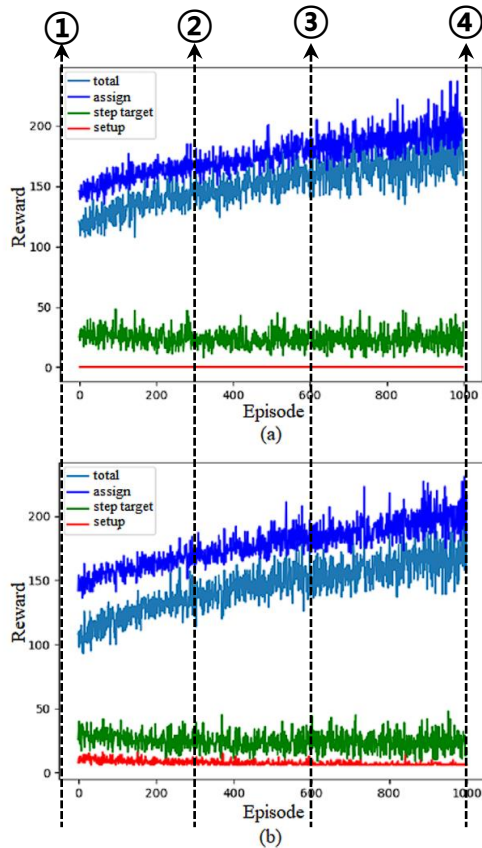


Fig. 5. Reward improvement in reinforcement learning (a) Experiment-A (b) Experiment-B.

에피소드 별 스케줄링 결과
→ 에피소드 진행됨에 따라 스케줄링 결과 최적화

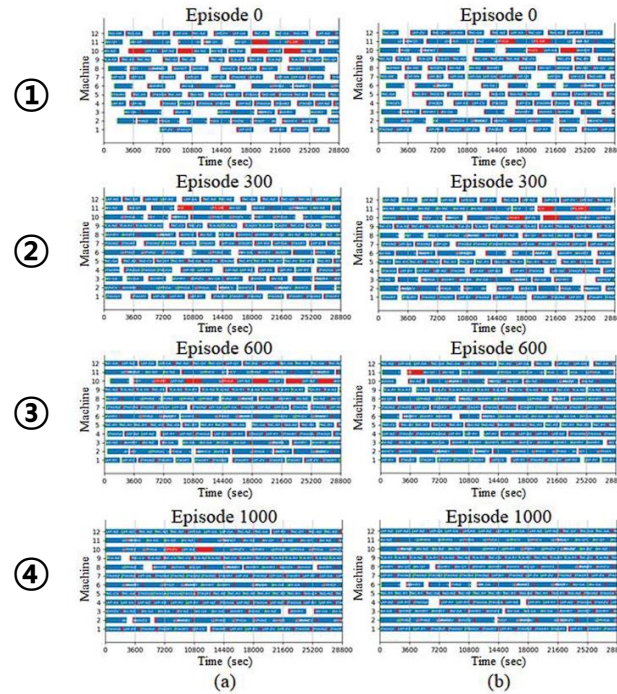


Fig. 7. Schedule Gantt chart with episodic learning. (a) Experiment-A (b) Experiment-B (blue: scheduled, red: setup, green: same lot type with previous job).

전반적으로 KPI Ratio > 1
→ 강화학습 기반에서 우수한 스케줄링 성과

$$\text{KPI Ratio} = \frac{\text{RLS (강화학습 기반 스케줄러)의 KPI}}{\text{RBS (규칙 기반 스케줄러)의 KPI}}$$

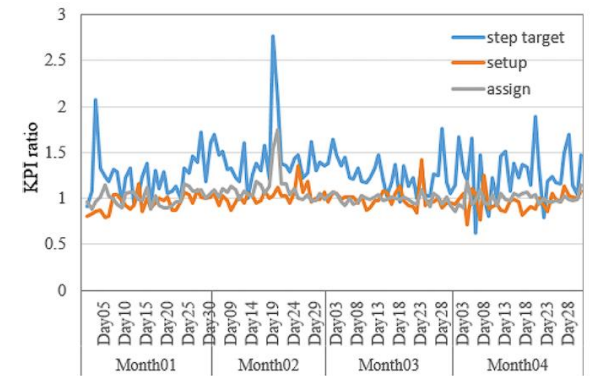


Fig. 8. KPI ratio between RLS and RBS. The numerator is the KPI of RLS and the denominator is the KPI of RBS.

TABLE VI
COMPARISON OF SCHEDULE PERFORMANCE

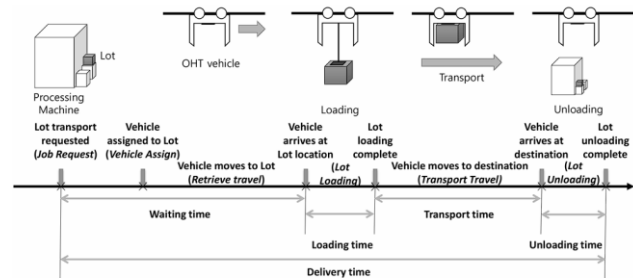
Item	step target	setup	assign
KPI ratio	1.311	0.985	1.036
Dominant rate	0.645	0.608	0.546
Equal rate	0.046	0.000	0.000
Inferior rate	0.308	0.392	0.454

3. 설비 스케줄링

각 설비의 가동 일정을 최적화하여 생산라인의 효율성을 높이고, 병목현상을 줄여 품질하락을 막고 생산 시간 단축

Case 1) 설비 → 다음단계 설비

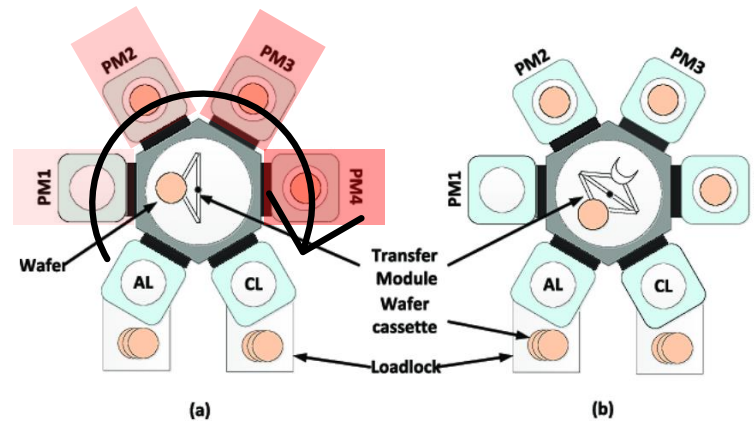
OHT : Overhead Hoist Transport



[6] Hong, S., Hwang, I., & Jang, Y. J. (2022). Practical q-learning-based route-guidance and vehicle assignment for oht systems in semiconductor fabs. IEEE Transactions on Semiconductor Manufacturing, 35(3), 385-396.

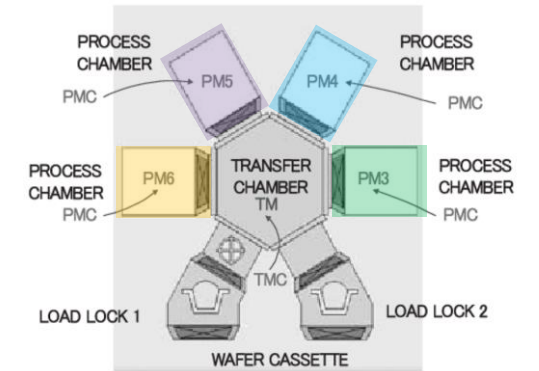
Case 2) 설비내 챔버/유닛 간 이동

- ① Cluster Tool : 여러 공정 단계를 순차적으로 수행
- ② Multi-Chamber Tool : 동일 기능 여러 유닛이 병렬로 구성



(a) Single-arm cluster tool; (b) Dual-arm cluster tool.

DOI: 10.1109/ACCESS.2021.3077503



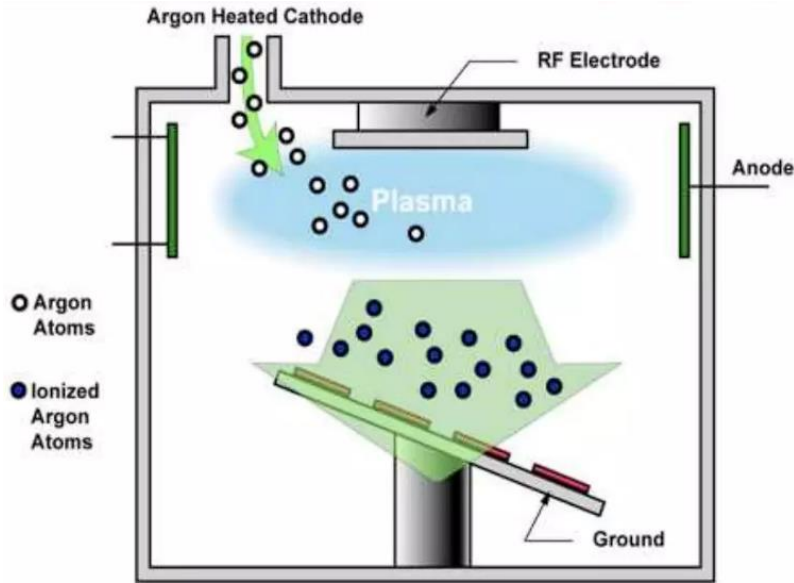
DOI:10.1541/IEEJIAS.124.160

Case 3) 검사/계측설비 – 한정된 설비 & 샘플링 검사

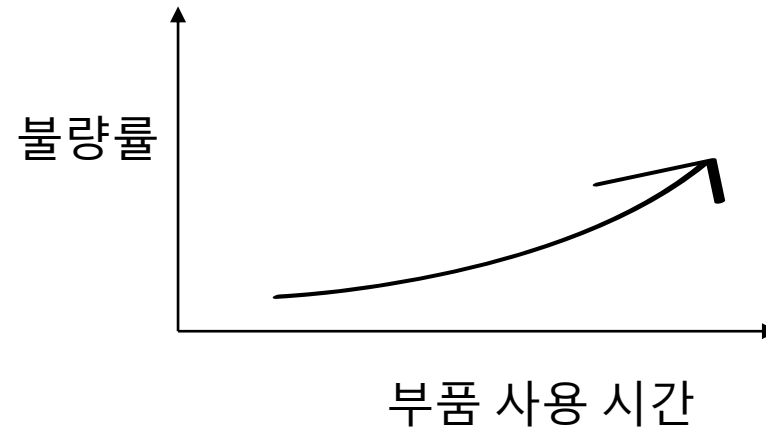
4. 부품 잔존수명 예측

설비의 주요 부품의 교체 시기를 예측하여 유지보수 시기를 미리 파악하고, 품질 저하를 막으며 예기치 않은 설비 고장을 방지

- ❖ **Multi-Scale and Multi-Branch Transformer Network for Remaining Useful Life Prediction in Ion Mill Etching Process (IEEE TSM, 2024)**



소모성 & 핵심 부품
→ 일정 기간 이상 사용 시 불량 유발
→ 핵심 부품 사용주기 관리 필요



Ion Milling Etching

: Ar 과 같은 비활성 기체를 이온화 하여 형성된 Ar+ 이온 빔을 사용하여 웨이퍼 표면에 충돌시켜 표면 물질을 제거

<https://www.slideshare.net/slideshow/ion-beam-etching-or-ion-milling-135052783/135052783>

4. 부품 잔존수명 예측

설비의 주요 부품의 교체 시기를 예측하여 유지보수 시기를 미리 파악하고, 품질 저하를 막으며 예기치 않은 설비 고장을 방지

❖ Multi-Scale and Multi-Branch Transformer Network for Remaining Useful Life Prediction in Ion Mill Etching Process (IEEE TSM, 2024)

Physical Feature	Formula Expression
Mean	$T_{i1} = \frac{\sum_{n=1}^N X_i}{N}$
Standard deviation	$T_{i2} = \sqrt{\frac{\sum_{n=1}^N (X_i - T_{i1})^2}{N-1}}$
Mean square amplitude	$T_{i3} = (\frac{\sum_{n=1}^N \sqrt{ X_i }}{N})^2$
Effective value	$T_{i4} = \sqrt{\frac{\sum_{n=1}^N (X_i)^2}{N}}$
Maximum	$T_{i5} = \max X_i $
Skewness	$T_{i6} = \frac{\sum_{n=1}^N (X_i - T_{i1})^3}{(N-1)T_{i2}^3}$
Kurtosis	$T_{i7} = \frac{\sum_{n=1}^N (X_i - T_{i1})^4}{(N-1)T_{i2}^4}$
Crest factor	$T_{i8} = \frac{T_{i5}}{T_{i4}}$
Margin factor	$T_{i9} = \frac{T_{i5}}{T_{i3}}$

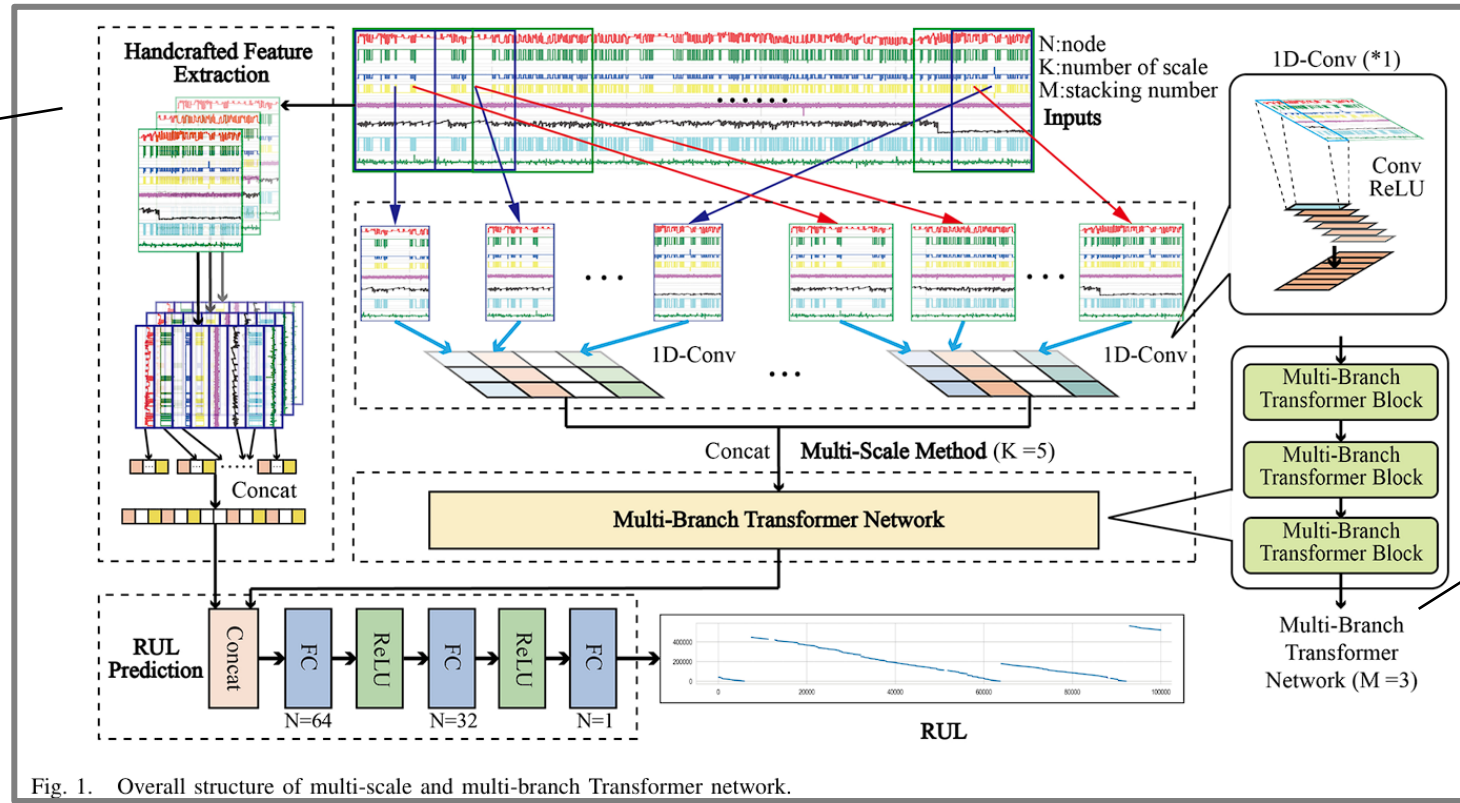


Fig. 1. Overall structure of multi-scale and multi-branch Transformer network.

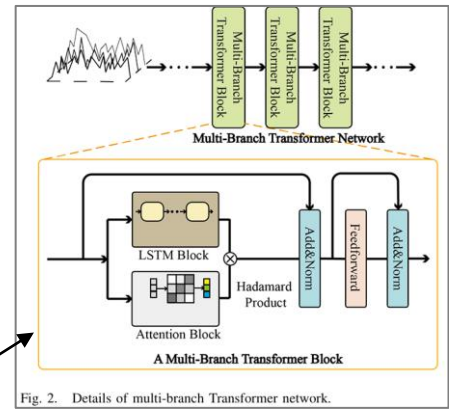


Fig. 2. Details of multi-branch Transformer network.

4. 부품 잔존수명 예측

설비의 주요 부품의 교체 시기를 예측하여 유지보수 시기를 미리 파악하고, 품질 저하를 막으며 예기치 않은 설비 고장을 방지

❖ Multi-Scale and Multi-Branch Transformer Network for Remaining Useful Life Prediction in Ion Mill Etching Process (IEEE TSM, 2024)

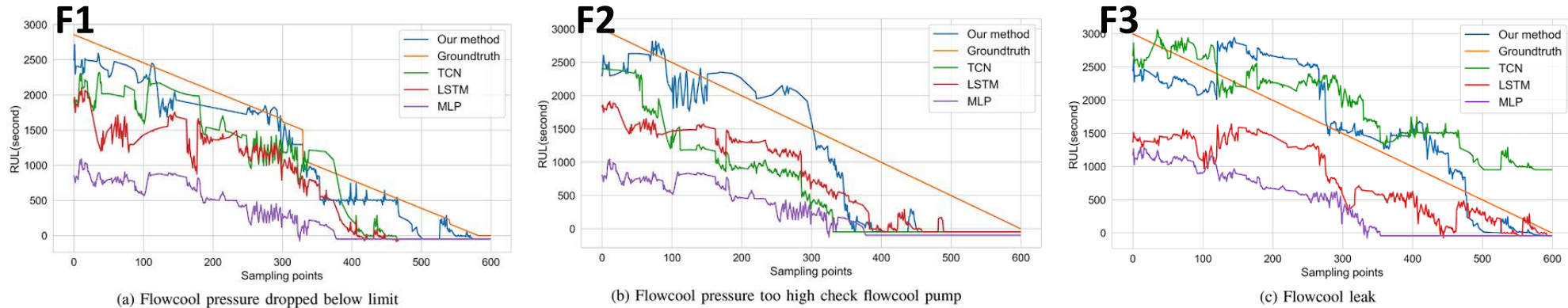


Fig. 7. RUL prediction results of three faulty modes in a run-to-failure cycle

TABLE IV
PERFORMANCE COMPARISON OF THREE FAULT MODES

Method	F1		F2		F3		Total number of parameters	Training Time_F1 (s)
	MAE	RMSE	MAE	RMSE	MAE	RMSE		
MLP	1484.75	1576.58	2179.04	2231.59	1604.44	1879.07	984,453	1507.437
LSTM-FCs	901.28	1026.72	1341.13	1637.65	1108.74	1335.87	1,194,497	2318.109
Bi-LSTM-FCs	877.42	1109.76	1136.07	1514.69	997.76	1275.35	2,649,601	4375.915
GRU-FCs	1043.17	1321.43	1577.09	1728.91	1097.23	1427.64	994,561	2147.752
Bi-GRU-FCs	912.21	1085.41	1291.05	1509.44	1008.43	1255.48	2,118,657	4491.034
CNN(VGG16-1D)	1282.29	1407.73	1796.65	1879.37	1347.71	1597.63	51,328,769	2264.499
TCN	789.65	932.21	1169.15	1312.67	967.71	1054.39	38,457,835	1974.055
Proposed method	567.21	646.42	676.71	798.29	597.78	691.31	1,525,882	2168.467

5. 원인인자 분석 & 수율 예측

제품 불량 원인을 찾아내고 생산 수율을 예측하여, 수율 향상을 위한 개선 방안 도출

❖ Commonality Analysis for Detecting Failures Caused by Inspection Tools in Semiconductor Manufacturing Processes (IEEE TSM, 2022)

반도체 제조공정에서의 Commonality Analysis ?

: Wafer가 진행된 이력(history)을 기반으로 특이한 불량 패턴을 갖는 wafer group 들의 공통점을 찾는 과정

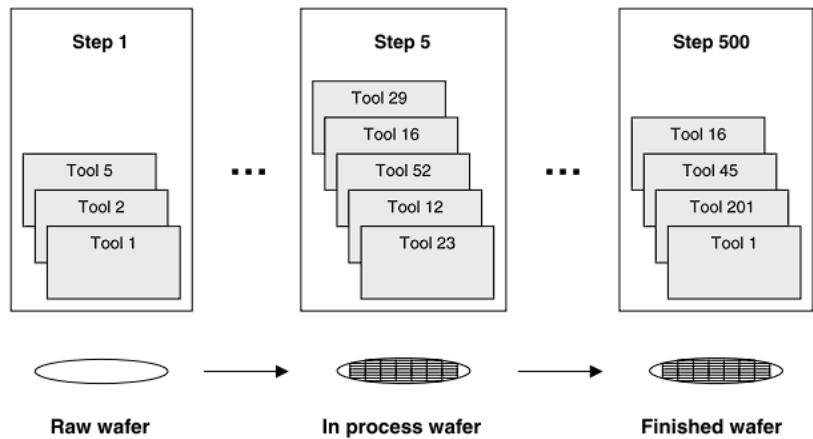


TABLE II
HISTORY LOG SCHEME

Wafer-ID	...	Step_(i,j,k)	Step_(i,j + 1,k)	...	Step_(i,j + m,k)	...	Yield	Binned_Yield
1	...	'Tool_129'	'Tool_239'	...	Null	...	70	'Bad'
2	...	'Tool_129'	'Tool_210'	...	Null	...	92	'Good'
3	...	'Tool_132'	'Tool_239'	...	'Tool_100'	...	94	'Good'
4	...	'Tool_141'	'Tool_210'	...	Null	...	72	'Bad'
...
N	...	'Tool_129'	'Tool_210'	...	'Tool_200'	...	73	'Bad'

[] Weiss, S. M., Baseman, R. J., Tipu, F., Collins, C. N., Davies, W. A., Singh, R., & Hopkins, J. W. (2010). Rule-based data mining for yield improvement in semiconductor manufacturing. *Applied Intelligence*, 33, 318-329.

5. 원인인자 분석 & 수율 예측

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❖ Commonality Analysis for Detecting Failures Caused by Inspection Tools in Semiconductor Manufacturing Processes (IEEE TSM, 2022)

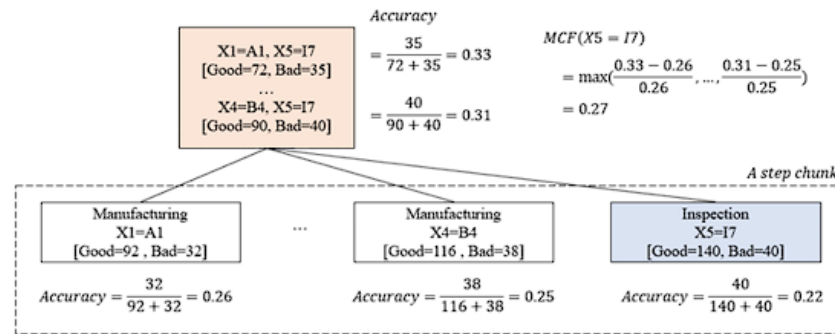


Fig. 1. An MCF calculation example.

MCF : Modified Cumulative factor

$$\begin{aligned}
 MCF(X) &= \frac{\text{Increase in accuracy by the manufacturing operation}}{\text{Accuracy of the inspection operation}} \\
 &= \max_{j \in \text{precedings}} \left(\frac{\text{accuracy}(A_j \cap X) - \text{accuracy}(A_j)}{\text{accuracy}(A_j)} \right) \\
 &= \max_{j \in \text{precedings}} \left(\frac{\text{support}(A_j \cap X, \text{'Bad'}) - \text{support}(A_j, \text{'Bad'})}{\text{support}(A_j, \text{'Bad'})} \right).
 \end{aligned} \tag{4}$$

Algorithm Commonality Analysis for Inspection Equipment

Input: data D ,
 binary threshold θ ,
 minimum-deviance δ ,
 significant level α

Output: O

Begin

Define 'Good', 'Bad' yield group from data D using θ

Define attribute set $A = \{A_1, A_2, \dots, A_i\}$ for all steps except yield from data D

Define equipment value set $V_i = \{V_{i1}, V_{i2}, \dots, V_{ij}\}$ for each attribute set A_i

Define contrast set C in conjunction with attribute and value set

Set of Candidates $P \leftarrow \emptyset$

1. **for each** $X \in C$ **do**
2. make contingency table for X
3. compute χ^2 static return p -value
4. compute $\text{support}(X, \text{'Bad'}) - \text{support}(X, \text{'Good'})$ return dev
5. **if** p -value $< \alpha$, $dev > \delta$ and X is inspection **then** Compute MCF(X)
6. **if** MCF(X) > 0 **then** $P \leftarrow X$
7. $O \leftarrow \text{SortValue}(\text{MCF}, p\text{-value}, dev)$

End

Fig. 2. Commonality Analysis for the Inspection Tool algorithm.

5. 원인인자 분석 & 수율 예측

제품 불량 원인을 찾아내고 생산 수율을 예측하여, 수율 향상을 위한 개선 방안 도출

❖ Commonality Analysis for Detecting Failures Caused by Inspection Tools in Semiconductor Manufacturing Processes (IEEE TSM, 2022)

불량 사례 – Case Study

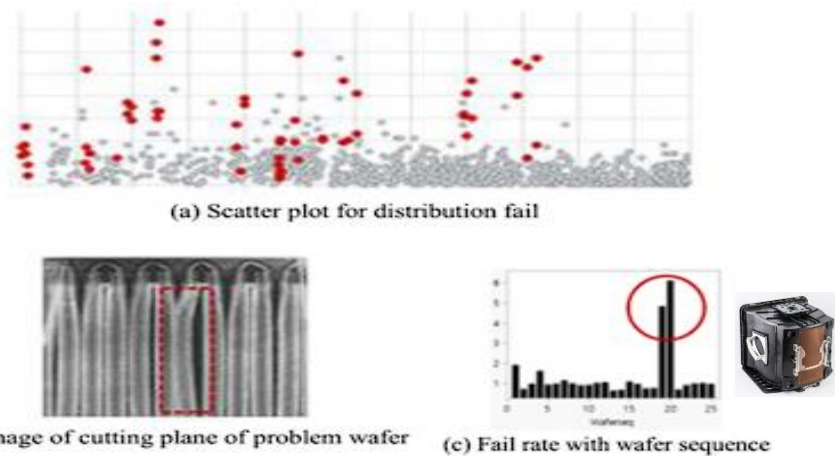


Fig. 4. A case of yield analysis in semiconductor fabrication.

TABLE VIII
LOG HISTORY FOR A CASE OF YIELD ANALYSIS IN FABRICATION

Wafer-ID	...	Inspection Step A	Manufacturing Step A	...	Inspection Step C	Manufacturing Step C	...	Group
1	...	Null	'2405'	...	Null	'1504'	...	'Good'
2	...	Null	'2405'	...	Null	'1504'	...	'Good'
3	...	'B902'	'2405'	...	'Null'	'1504'	...	'Bad'
4	...	'B902'	'0501'	...	'0202'	'1504'	...	'Bad'
...	'1504'
2797	...	'4001'	'2405'	...	Null	'1504'	...	'Good'

TABLE X
COUNT OF THE BAD GROUP IN THE INSPECTION STEPS AND THE MANUFACTURING STEPS (IN THE RESULTS OF THE EXPERIMENT OF ALGORITHM PERFORMANCE)

(A) INSPECTION STEP A			
Inspection Tools	Manufacturing Tools	Wafer Count	Abnormality
4001	2405	5	
B902	0501	25	.91
B902	2405	27	
(B) INSPECTION STEP C			
Inspection Tools	Manufacturing Tools	Wafer Count	Abnormality
Null	1504	23	
0202	1504	32	.56
0701	1504	2	
(C) INSPECTION STEP K			
Inspection Tools	Manufacturing Tools	Wafer Count	Abnormality
1902	E506	10	1.00
1902	E509	47	
(D) INSPECTION STEP B			
Inspection Tools	Manufacturing Tools	Wafer Count	Abnormality
D202	2108	13	1.00
D202	2110	44	
(E) INSPECTION STEP G			
Inspection Tools	Manufacturing Tools	Wafer Count	Abnormality
1902	0702	57	1.00

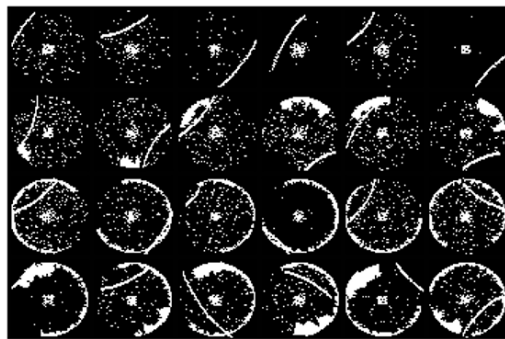
most suspicious step

proposed method
MCF

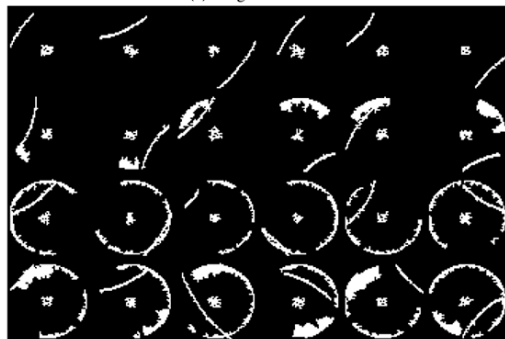
6. 웨이퍼 맵

반도체 웨이퍼 맵의 불량 발생 패턴을 분석하여 불량 개선의 인사이트를 발굴

❖ Semi-Supervised Learning for Simultaneous Location Detection and Classification of Mixed-Type Defect Patterns in Wafer Bin Maps (IEEE TSM, 2022)



(a) Original WBMs



(b) Filtered WBMs

Fig. 4. (a) Examples of mixed-type defect patterns. (b) WBMs after removing random defects using the CPF filtering method.

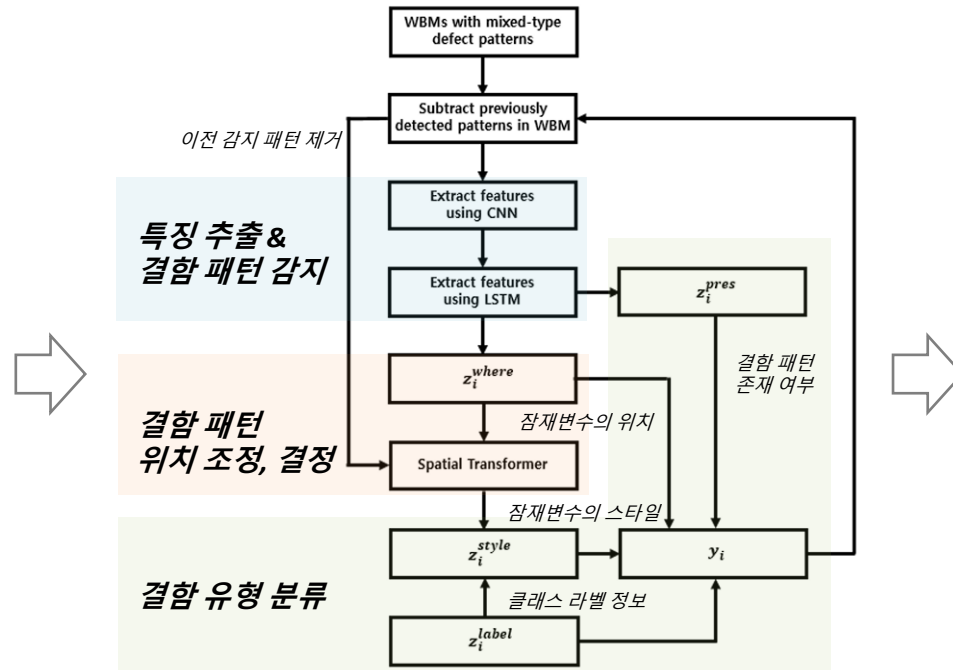


Fig. 2. Flow chart for SS-AIR for simultaneous location detection and classification of mixed-type defect patterns in WBMs. The process is repeated for $i = 1, \dots, n$.

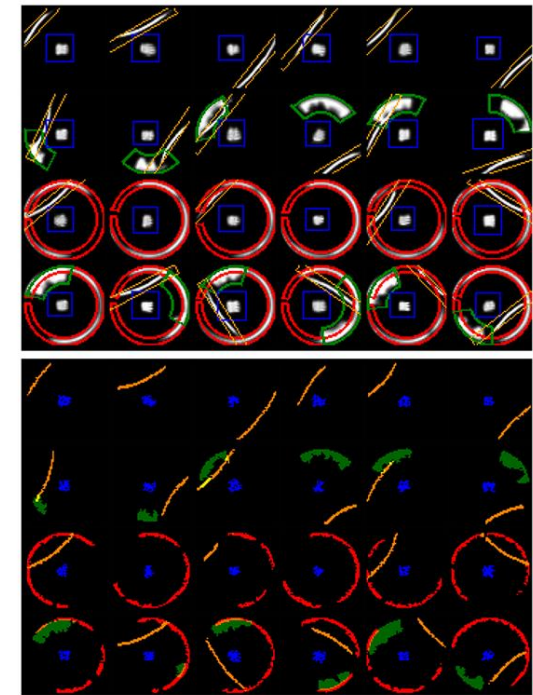
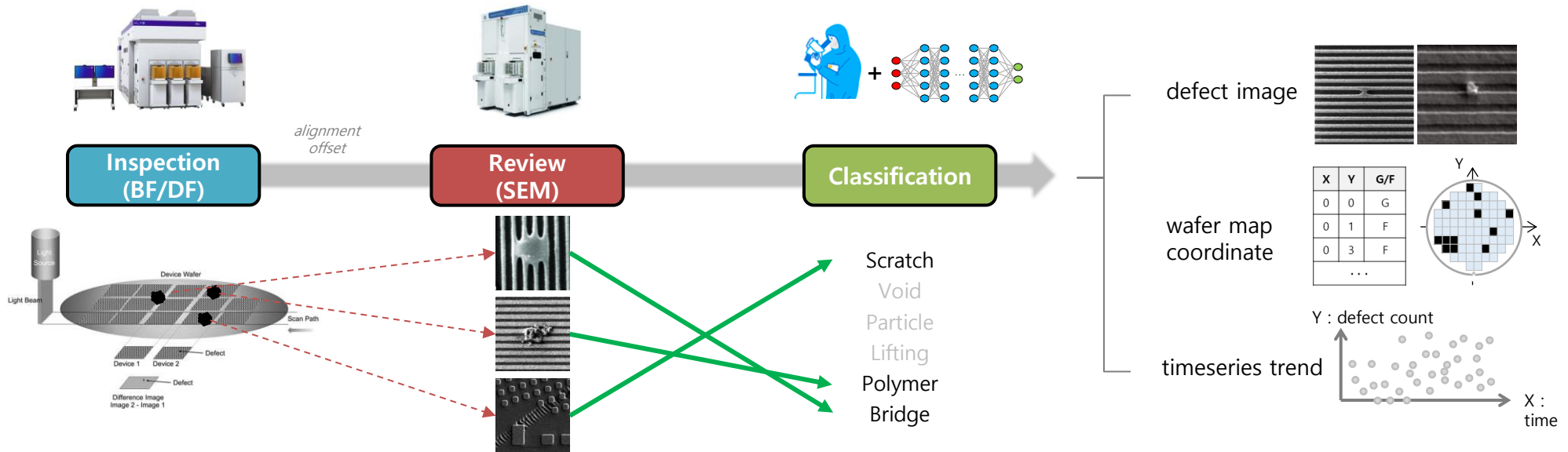


Fig. 7. Detected locations of defect patterns using SS-AIR with the proposed pattern-specific cropping mechanisms (top) and the patterns of partial ring, scratch, local zone, and center circle represented by red, orange, green, and blue, respectively (bottom).

7. 검사/리뷰/분류

검사 공정의 자동화 및 정밀도 향상을 통해 불량을 신속하고 정확하게 찾아내고 분류

➤ 반도체 제조공정 중 검사공정 프로세스



1 Inspection

- 각 칩의 정상/결함 판정
- Object Detection
- Offset/Alignment
- Nuisance Rate

2 Review

- 결함 이미지 촬영 & 이미지화
- Super Resolution
- Image Processing/Enhancement
- Object Detection
- Image Segmentation

3 Classification

- 결함의 클래스 분류
- Auto Defect Classification (ADC)

7. 검사/리뷰/분류

검사 공정의 자동화 및 정밀도 향상을 통해 불량을 신속하고 정확하게 찾아내고 분류

- ❖ Precise **Pattern Alignment for Die-to-Database Inspection** Based on the **Generative Adversarial Network** (IEEE TSM, 2022) (D2DB)

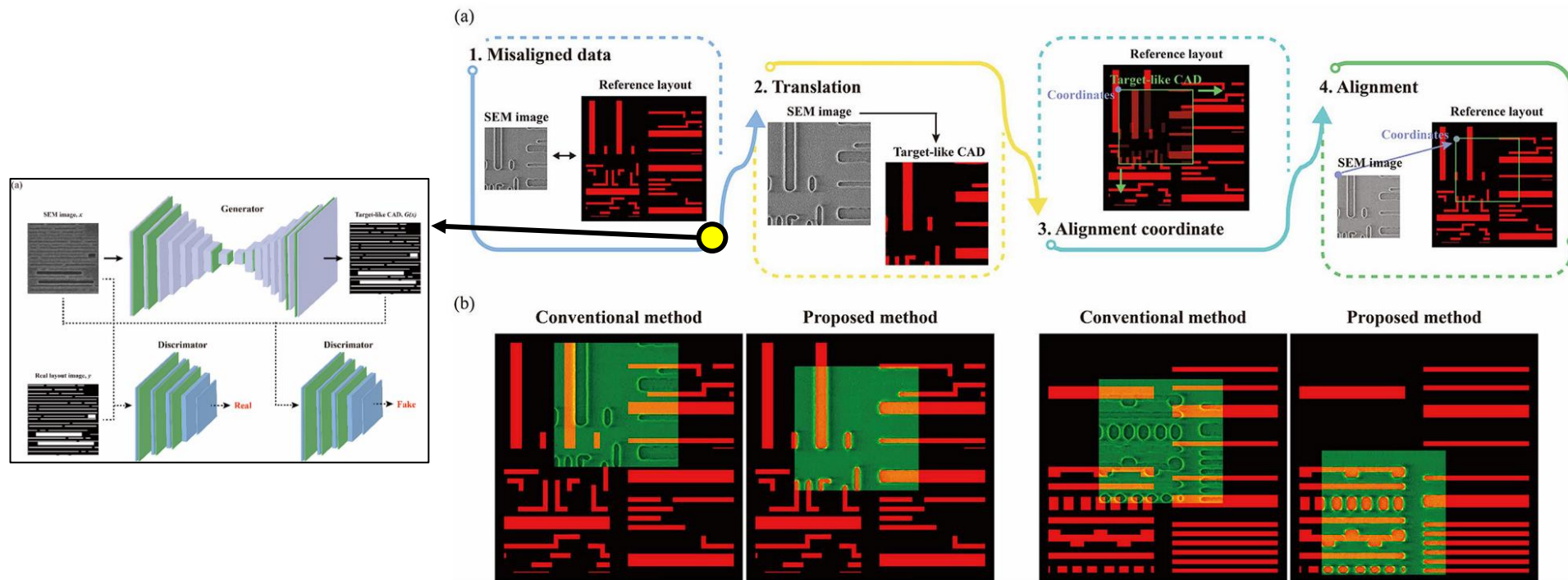


Fig. 1. Brief introduction of the proposed alignment framework. (a) Graphical explanation of the proposed approach. The SEM image is translated into the target-like CAD image. Then, alignment is conducted between the translated target-like CAD image and the reference layout to obtain the alignment coordinates. Finally, the SEM image is placed to the alignment coordinates of the reference layout. (b) Comparison of alignment results between the conventional method and the proposed method.

3. Summary & Conclusion

Summary & Conclusion

- ✓ 학계, 빅테크 기업 주도로 진행되는 인공지능 기술의 발전과 함께, 각 산업계에서는 AI기술을 어떻게 활용할지에 대한 다양한 고민 중
- ✓ 제조업에서도 AI 활용에 대한 수요 높음

- ✓ 반도체 제조공정 분야 저널, 학회에서 2022년 이후 발표된 연구주제 탐색 → 대표 연구분야
: IEEE Transactions on Semiconductor Manufacturing(IEEE TSM)
: Annual SEMI Advanced Semiconductor Manufacturing Conference(ASMC)

- ✓ 주어진 문제 상황에 대해 범용적이고 안정적인 딥러닝 모델을 사용하면서도 도메인 지식을 적절하게 결합하여 원하는 결과를 도출

- ✓ 산업현장에 적용을 위해서는 인공지능 지식 뿐만 아니라 도메인 지식과 문제상황을 충분히 이해한 상태에서 문제를 풀어나갈 수 있어야 함

고맙습니다.